



**PERÚ**

Ministerio  
del Ambiente

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Geofísico del Perú - IGP

Dirección  
Científica

Radio Observatorio  
de Jicamarca

# **JRO: R&D (IDI) Acquisition Systems**

**Joaquín Verástegui**  
**2018**

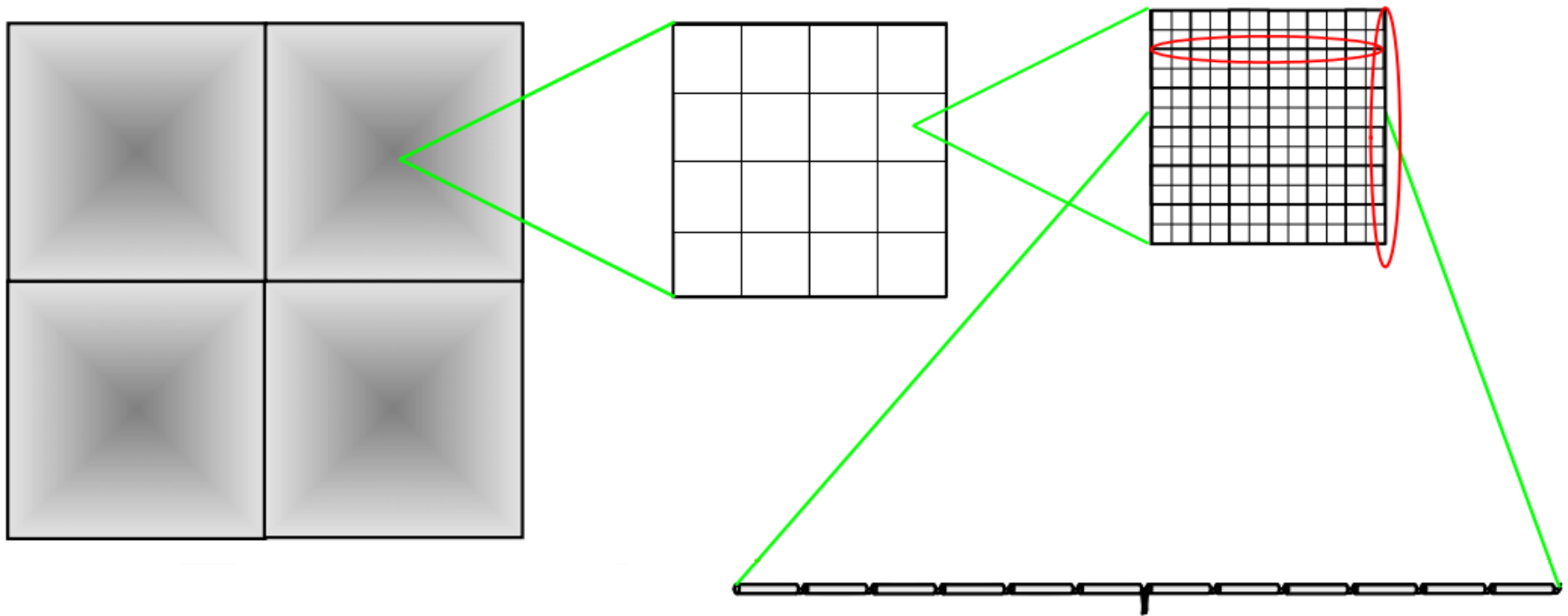


# Main Radar

- Located 20 Km North of Lima
- 18,432 dipoles
- Area: 85,000 m<sup>2</sup>
- Working frequency 49.92 MHz
- 6MW Power (4 Tx, each 1.5 MW)



# Antenna



# How do we get radar data?

Step 1: Get Radar

Step 2: Magic

Step 3: Data!



# How do we get radar data?

## Step 1: Get Radar

- RF signal, Amps, Tx, T/R, Antenna, Rx

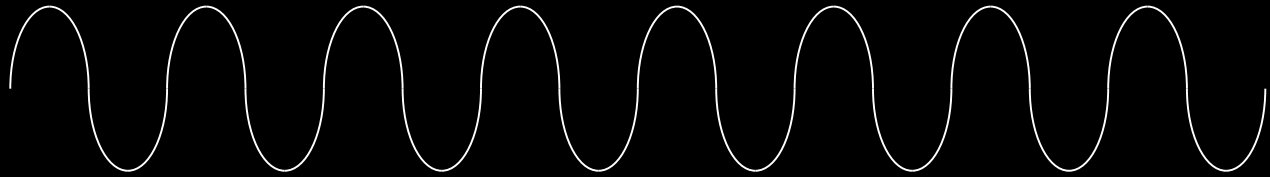
## Step 2: Magic

- Digital Synthesizer, Radar Controller, Data Acquisition System, Monitoring, Visualisation, Pre Processing, Storage

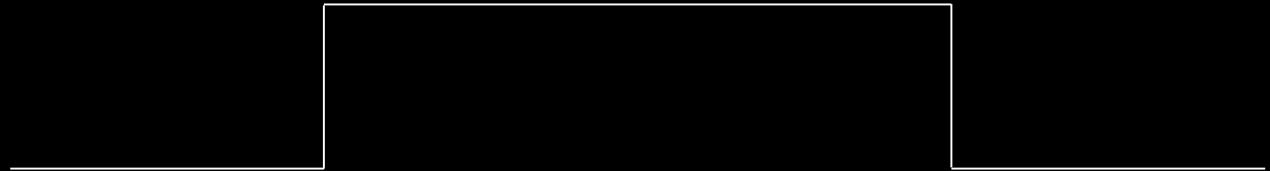
## Step 3: Data!

# System Block Diagram

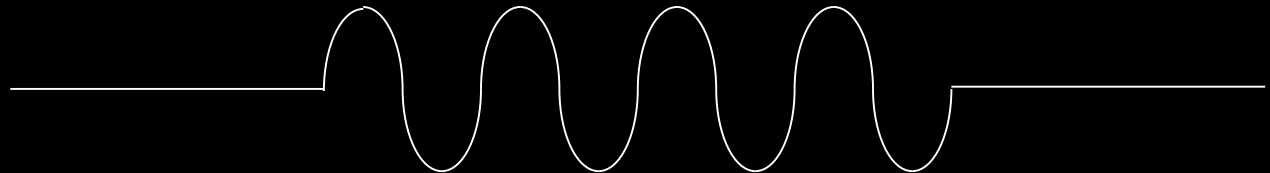
**RF Signal**



**ASK  
modulating  
Signal**



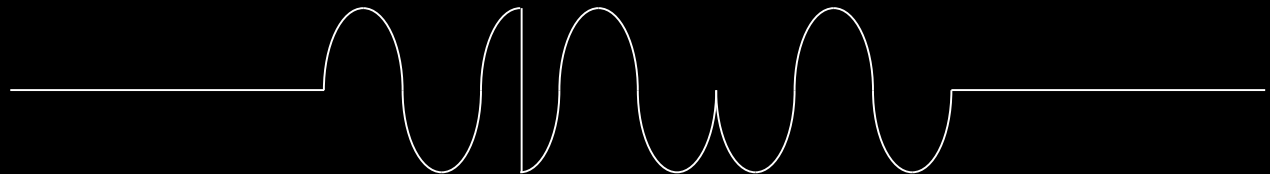
**RF  
modulated  
Signal**



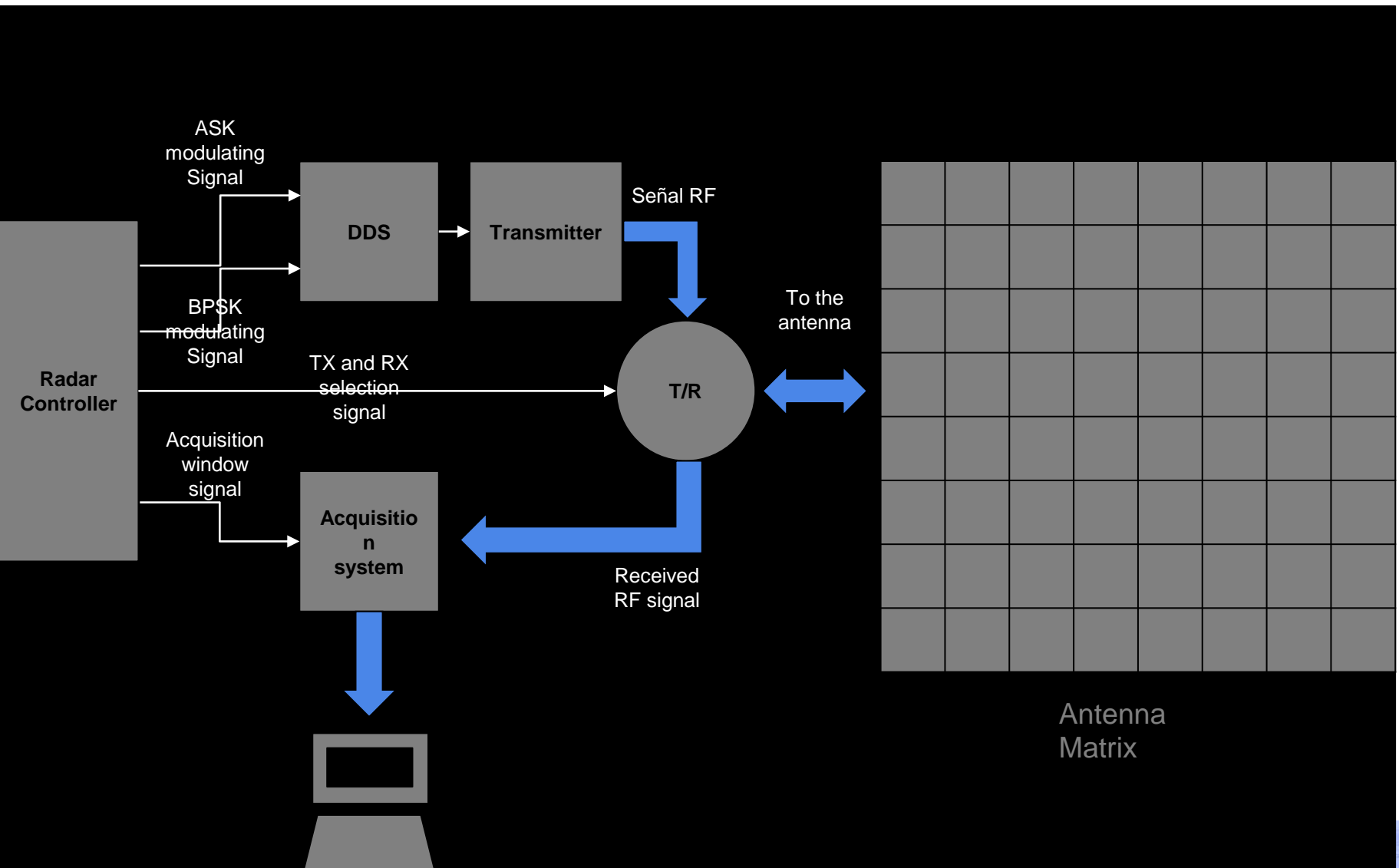
**BPSK  
modulating  
Signal**



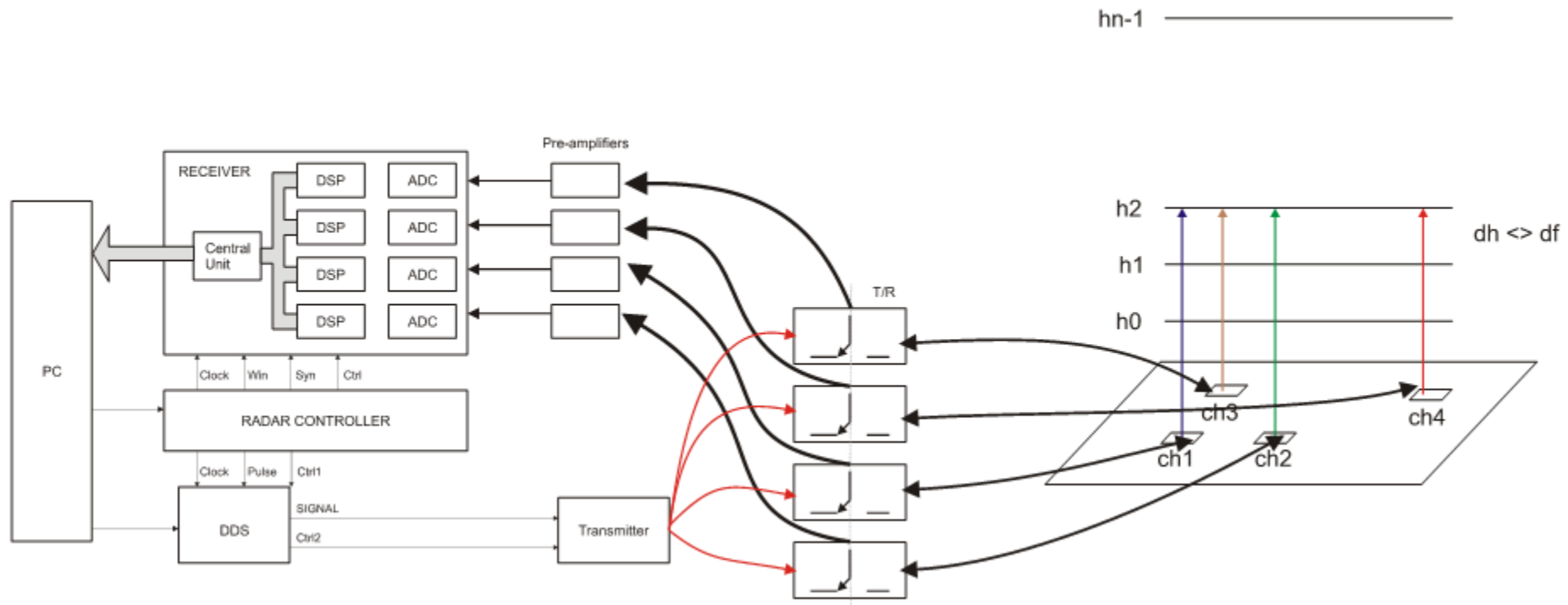
**RF  
modulated  
Signal**



# System Block Diagram



# System Block Diagram

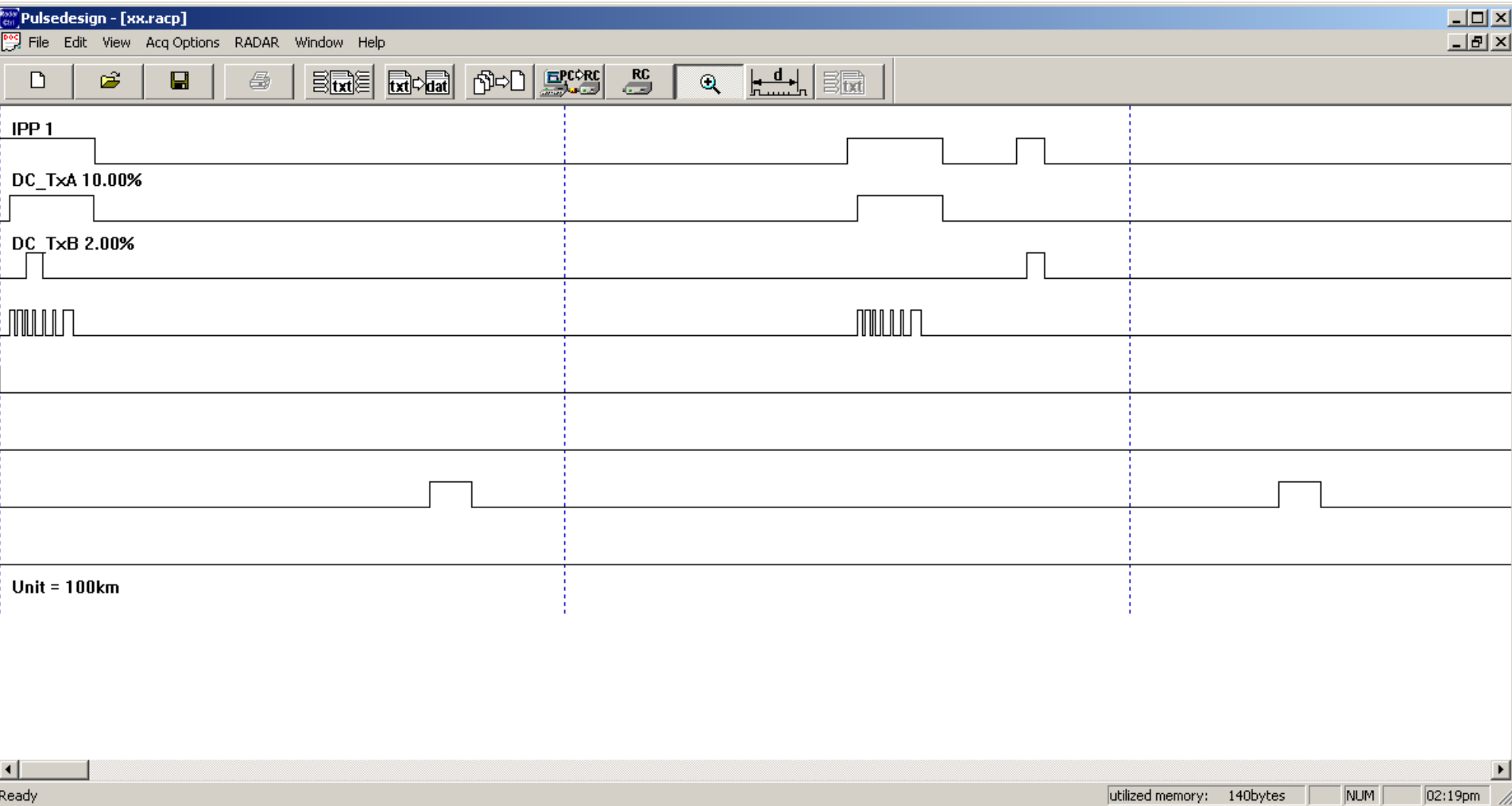




# 1. Radar Controller (CR)



# Radar Controller - Pulse Design



# Radar Controller - Pulse Design



▼ Radar Controller Parameters

▼ Inter Pulse Period (IPP)

Inter Pulse Period

1400.000

28000

units

km

Pulse RF

107.14286

Hz

▶ Number of Pulse to transmit & Pulse Selection

▶ Transmitter A (TXA)

▶ Transmitter B (TXB)

▶ Code A (Code Entries)

▶ Code B (FLIP 1)

▶ Code C (FLIP 2)

▶ Code D (Sample Window Characteristics)

▶ Controller Settings

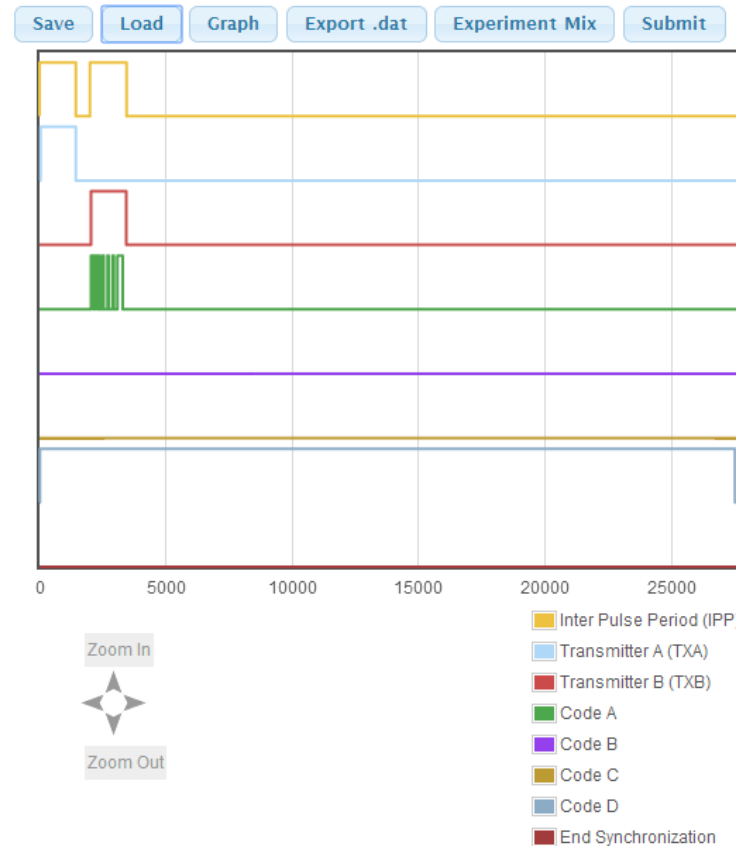
▶ Special Settings

▶ Control Switches (Ctrlr1 Ctrlr2)

▶ CLOCK

▶ Process Parameters

▶ Console Log



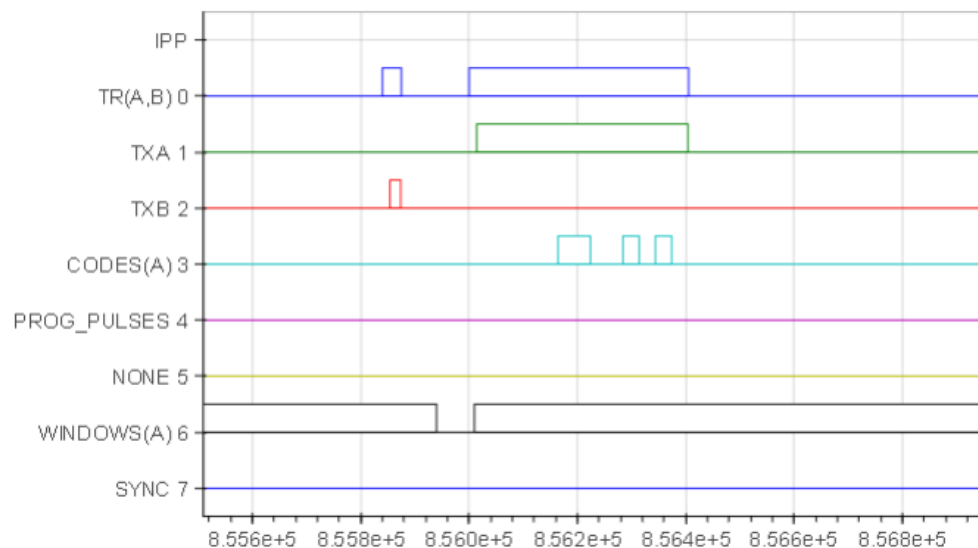
# Radar Controller - Pulse Design



## RC Pulses Imaging [2016/07/06]



+ | 0P | ↺ | 📄 |



Axis

Units

1 Km 8.0 Units

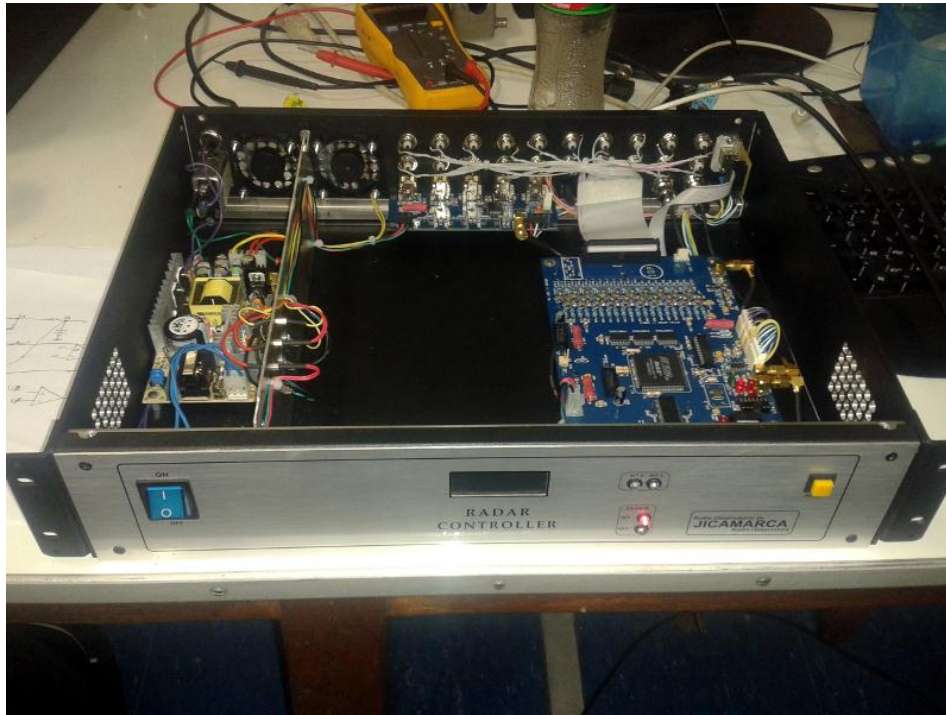
1 Unit 0.125 Km

# Radar Controller - V 1.0 USB



- CPLD
- 8 Channel
- Programmed by USB

# Radar Controller - V 1.1 USB



- CPLD
- 8 Channel
- Programmed by USB
- Increased resilience to EM interference from circuitry, clock



# Radar Controller - V 2.0

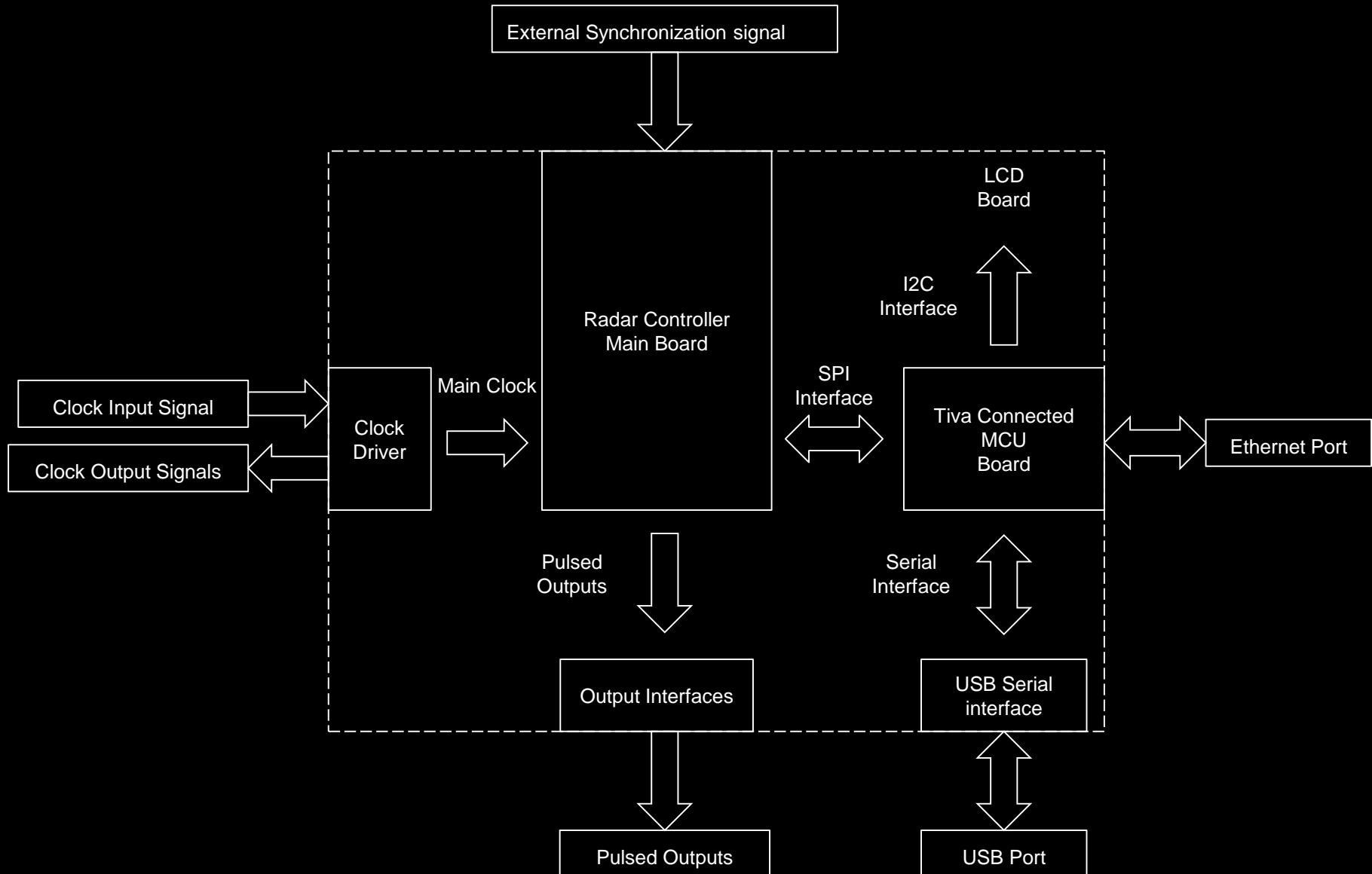
## Ethernet



- Spartan 6 FPGA
- 16 programmable channels
- Additional Memory
- Programmed by Ethernet
- Backward USB compatibility
- Real-time

monitoring of  
signals

# Radar Controller - V 2.0 Ethernet

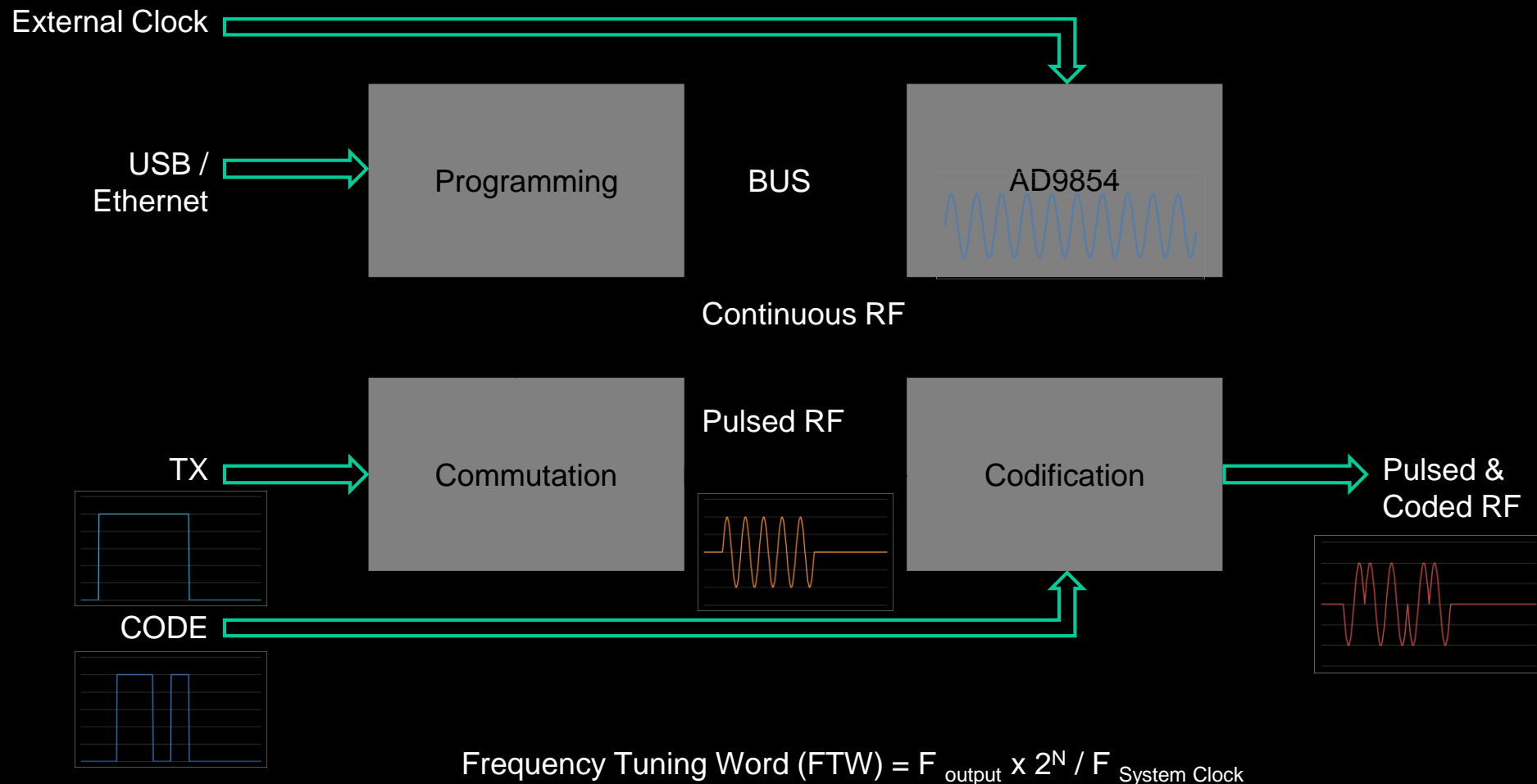




## **2. Direct Digital Synthesizer (DDS)**



# Direct Digital Synthesizer (DDS)



# Direct Digital Synthesizer (DDS)



- 48-bit resolution
- 4x Multiplier
- 2 Channels
- 60dB crosstalk
- Programmed by USB / Ethernet

# Direct Digital Synthesizer (DDS)



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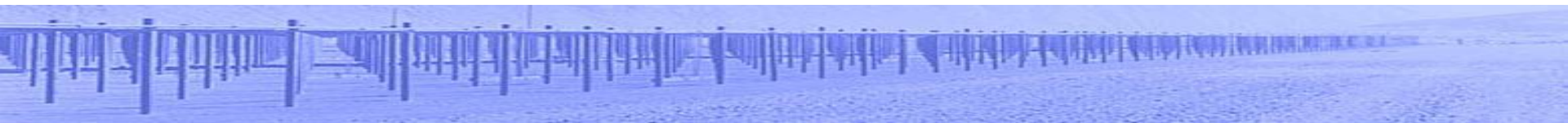
Device Configurations

## DDS Configuration Details

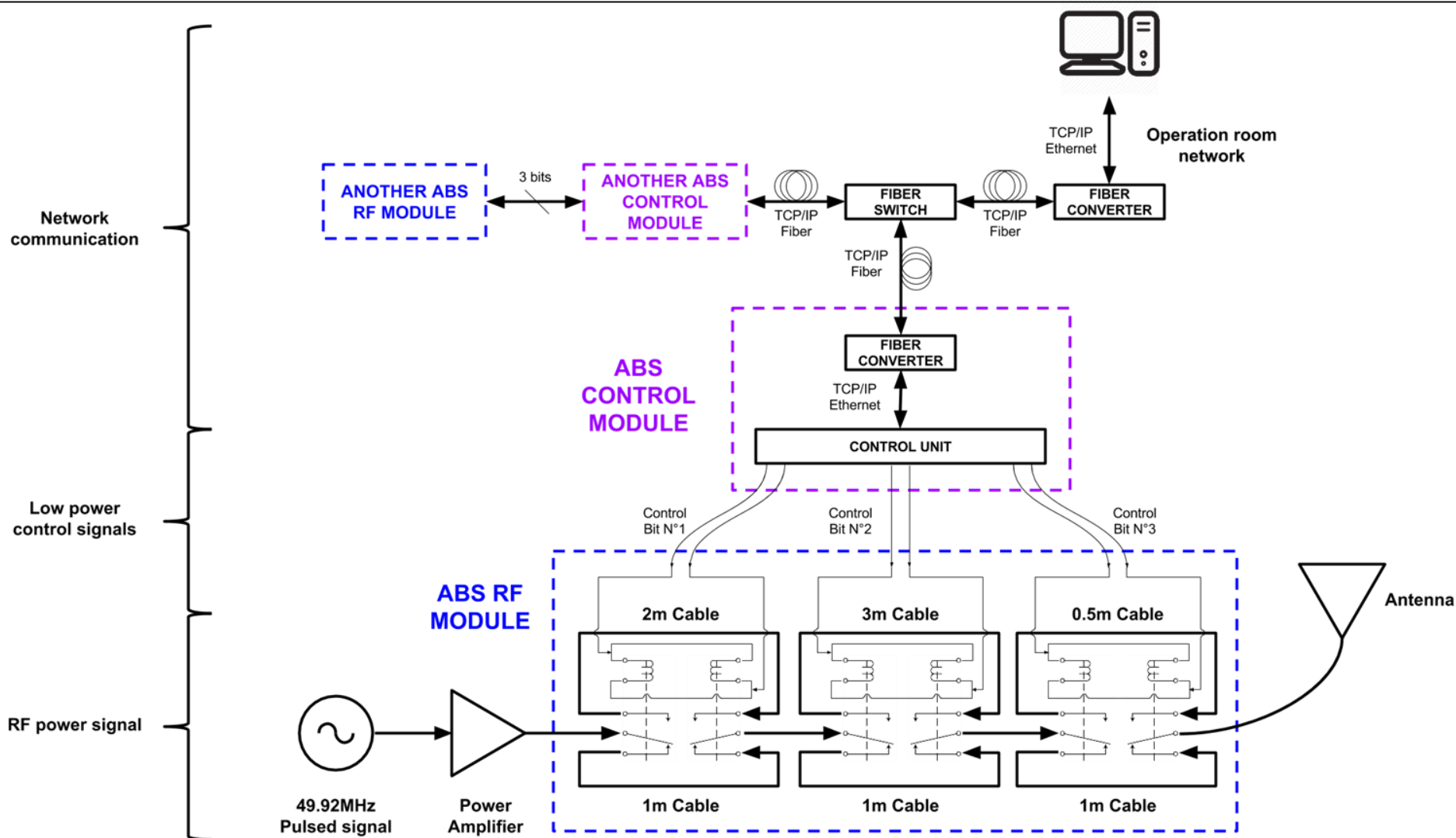
Status	⊗ No connected
Configuration Name	DDS: DDSv2 (pruebas IDI)
Clock In (MHz)	60.0
Multiplier	4
Frequency A (MHz)	39.9359999969576052
Frequency A (Decimal)	46837436121085
Frequency B (MHz)	0.0000000000000000
Frequency B (Decimal)	0
Phase A (Degrees)	0.0
Phase B (Degrees)	0.0
Modulation Type	Single Tone
Amplitude Control	Enabled
Amplitude CH1	1000
Amplitude CH2	1000

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### **3. ABS (Automatic Beam Stearing)**



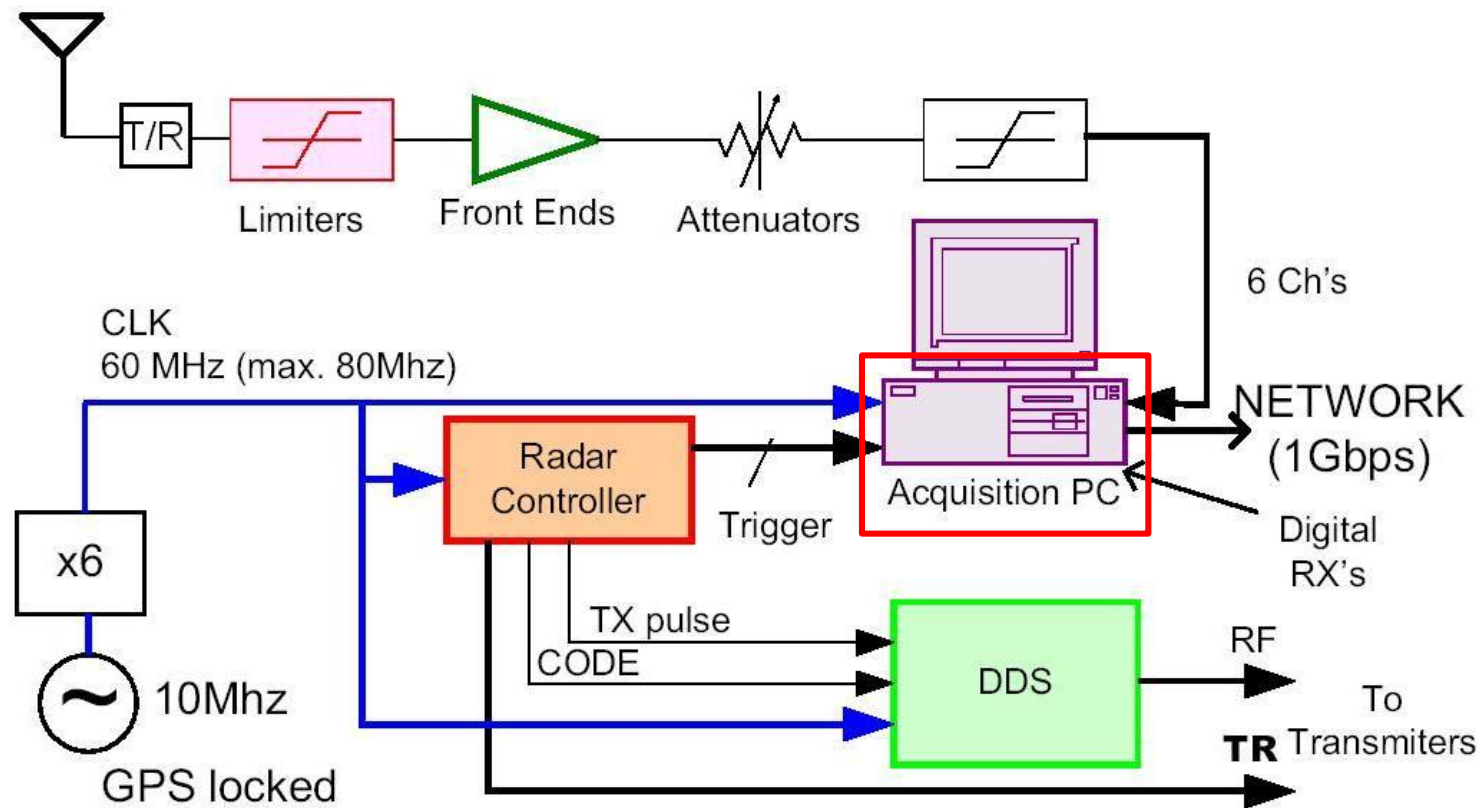
# ABS Diagram



## 4. JARS (JRO Acquisition Radar System)

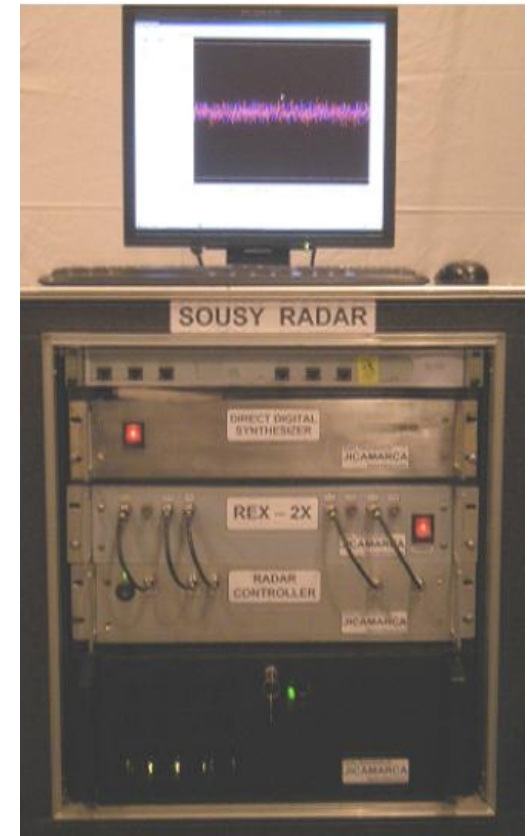
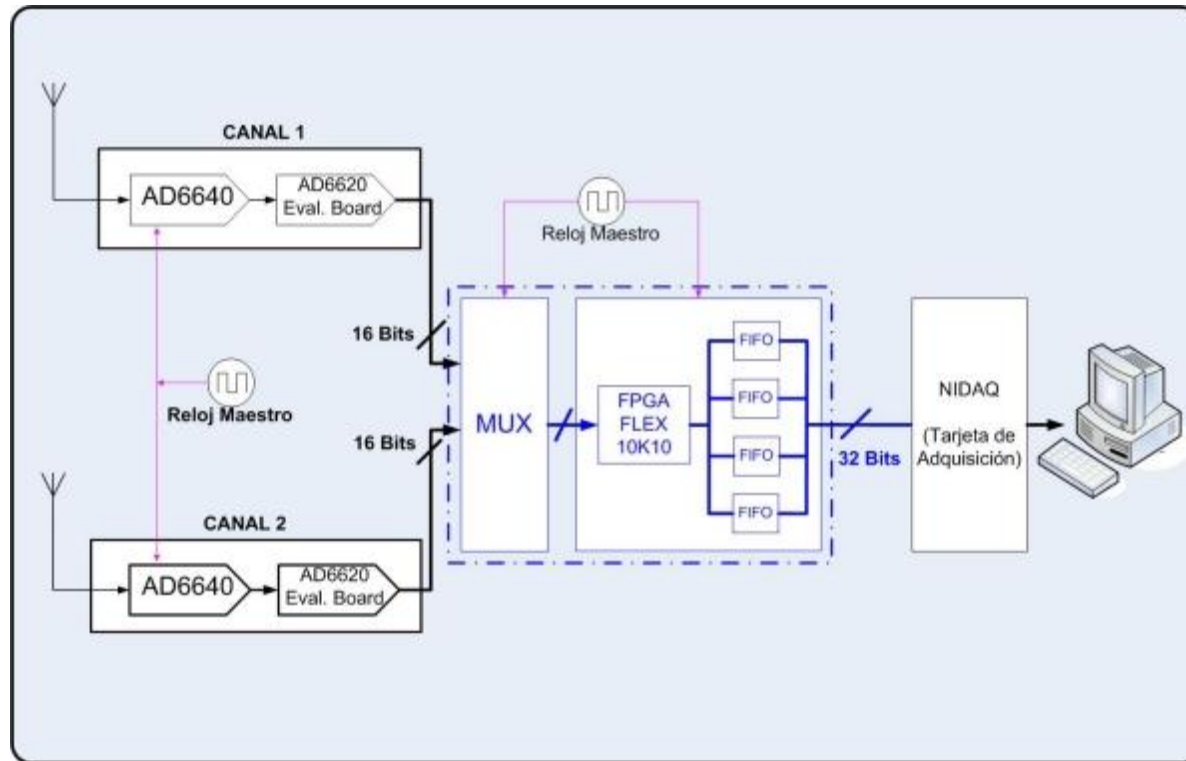


# Acquisition system using ECHOTEK Digital Receiver





# REX2 Reception System using AD6620 digital receiver



# JARS 1 (JRO Acquisition Radar System)



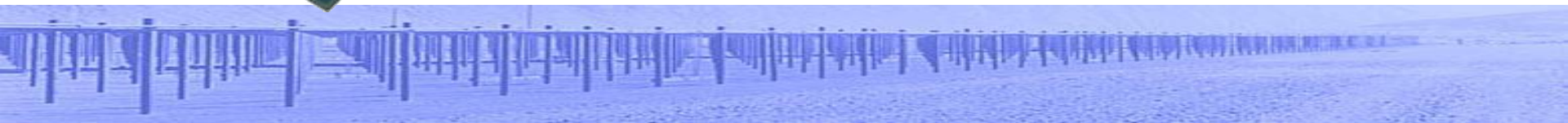
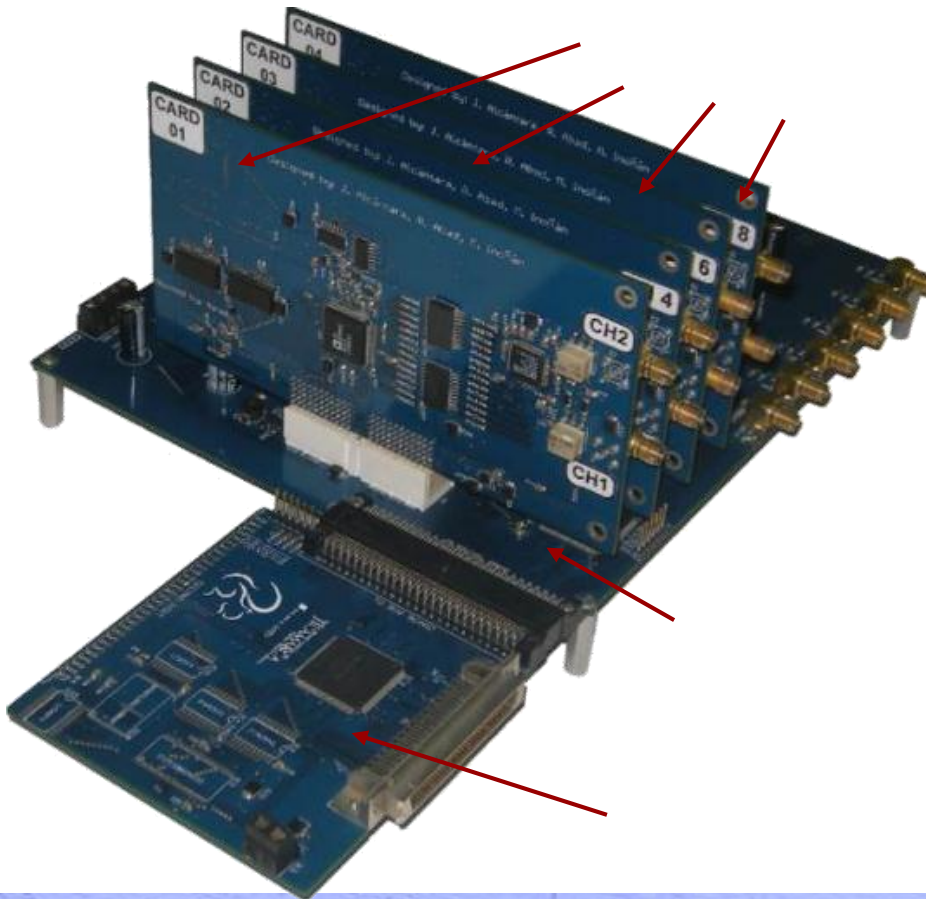
# JARS characteristics

- 8 channels system.
- 60MHz main clock.
- Based on three Altera MAXII CPLD.
- Based on National Instruments NiDAQ acquisition system with PCI connection.
- Dynamic range: 80dB.
- Bandwidth in baseband per channel: 4MHz using one channel and 1MHz using eight channels.
- Decimation range: 4 to 16384.
- Full scale voltage: 1.41Vpp @ 50 ohm.

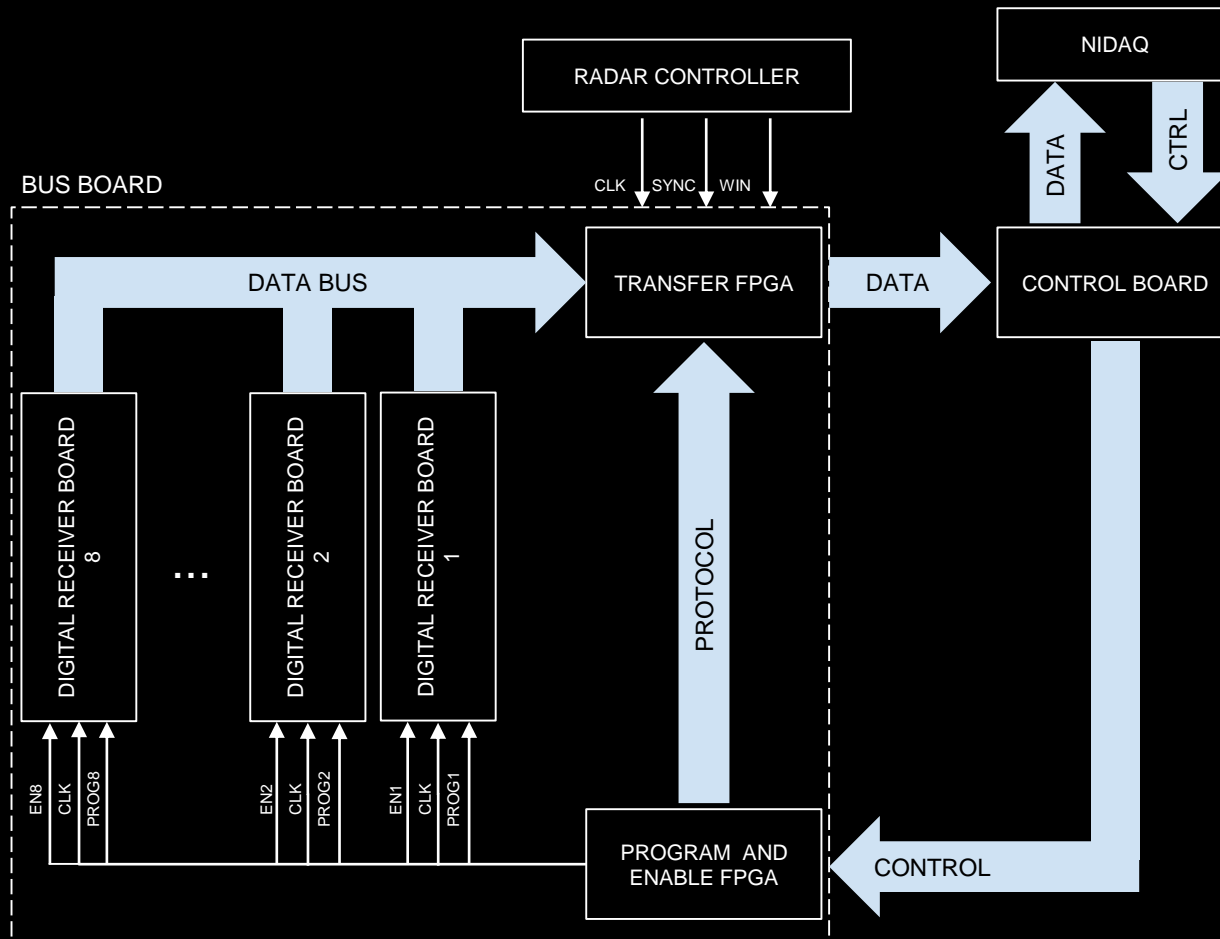




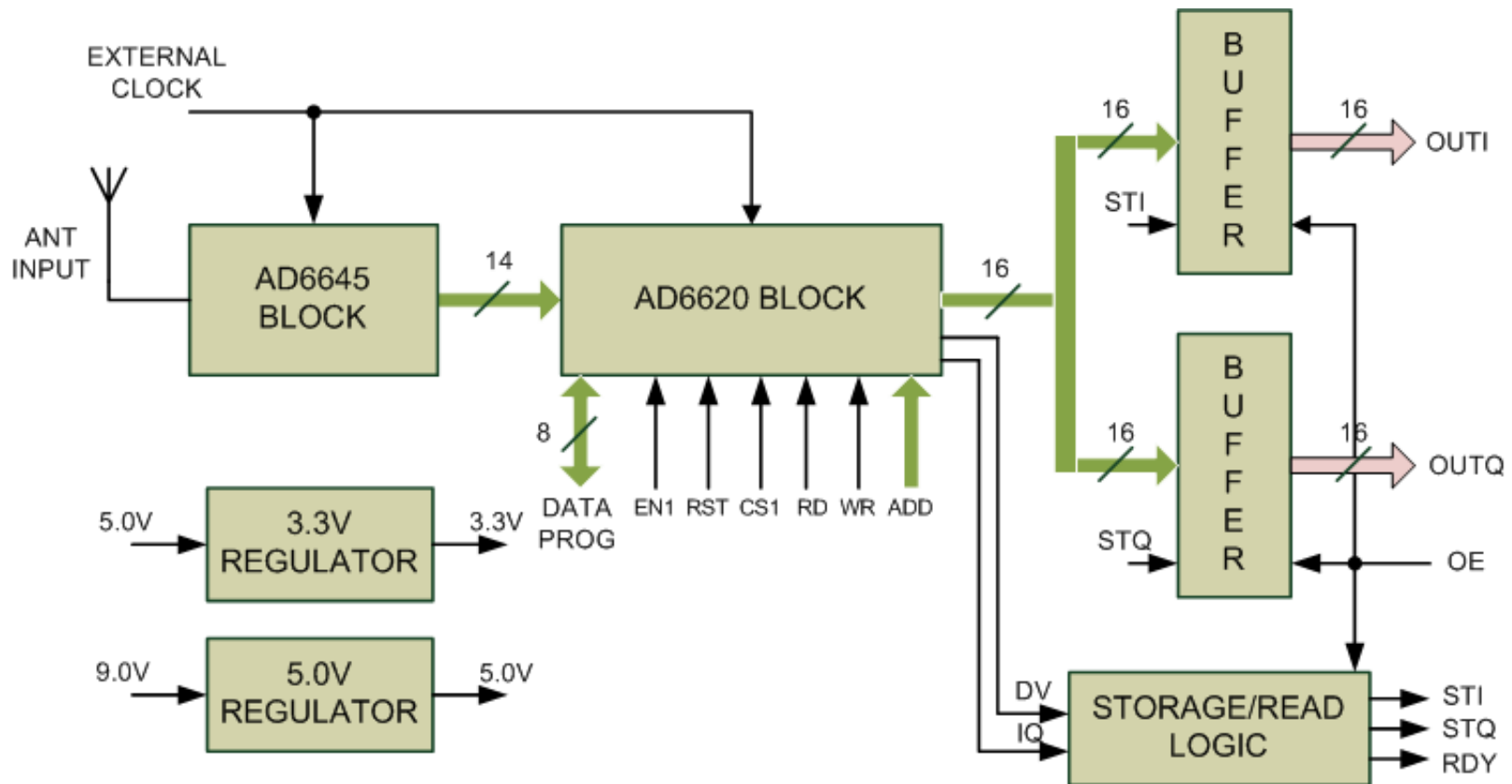
# JARS system



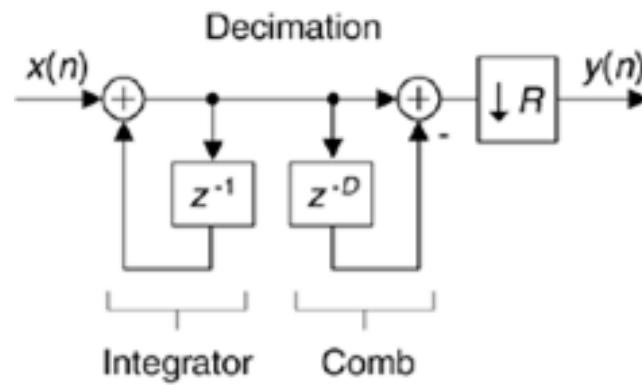
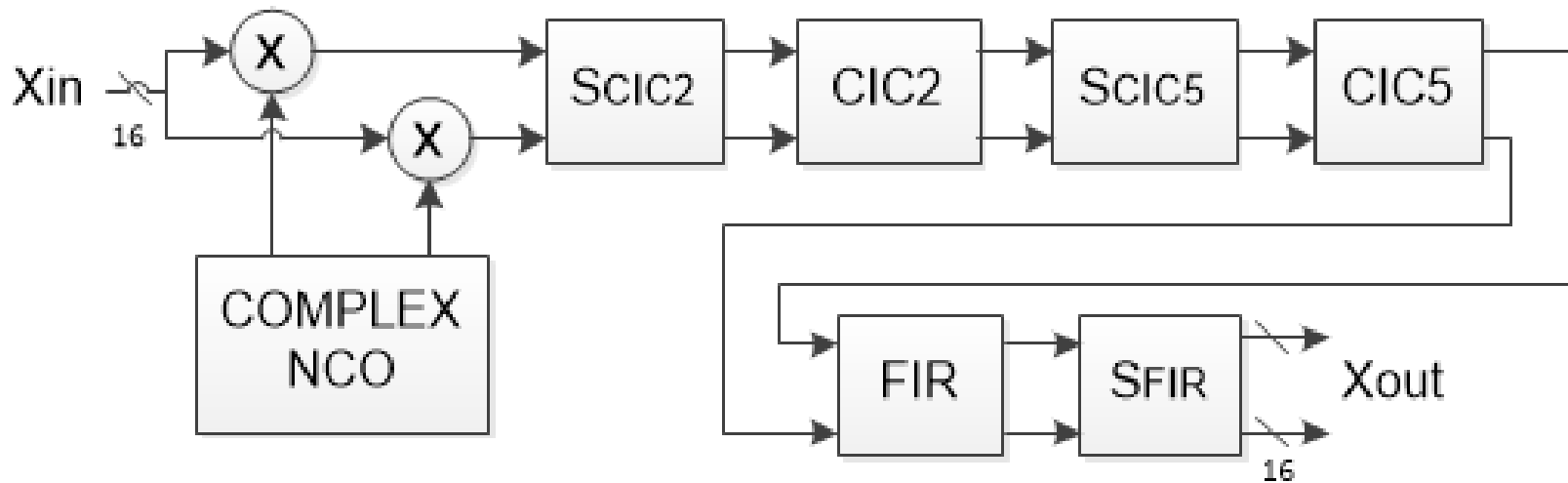
# JARS system



# Digital receiver design

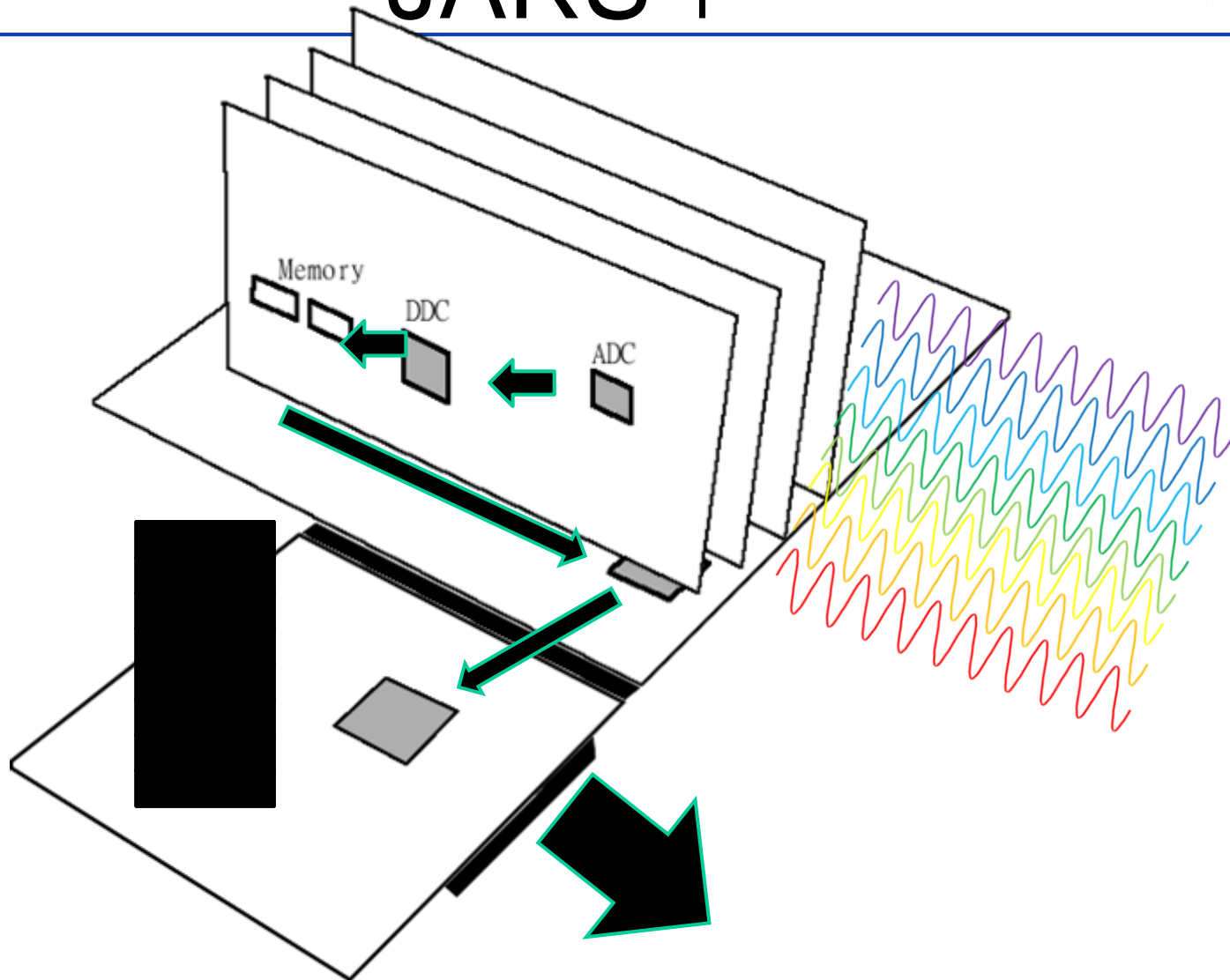


# AD6620 design



(a)

# JARS 1





# JARS 1



# JARS 1



- 8 Channel
- 60 MHZ clock
- CPLD
- NiDAQ Connection to PCI Express



# JARS 1

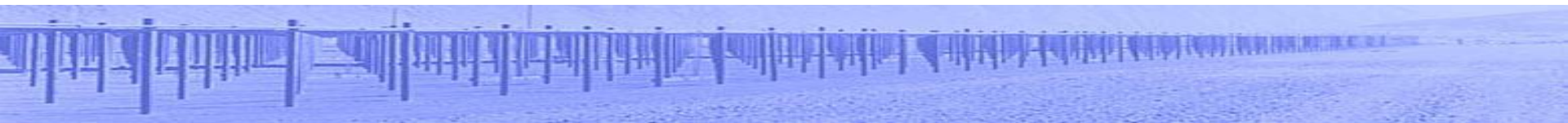


## ADC (Analog to Digital Converter)

- 14 bits
- 500ps aperture delay

## DDC (Digital Down Converter)

- 32 bits NCO (Numerically Controlled Oscillator)
- 2 CIC (Cascaded Integrator–Comb) and 1 FIR (Finite Impulse Response) filter





# JARS 1



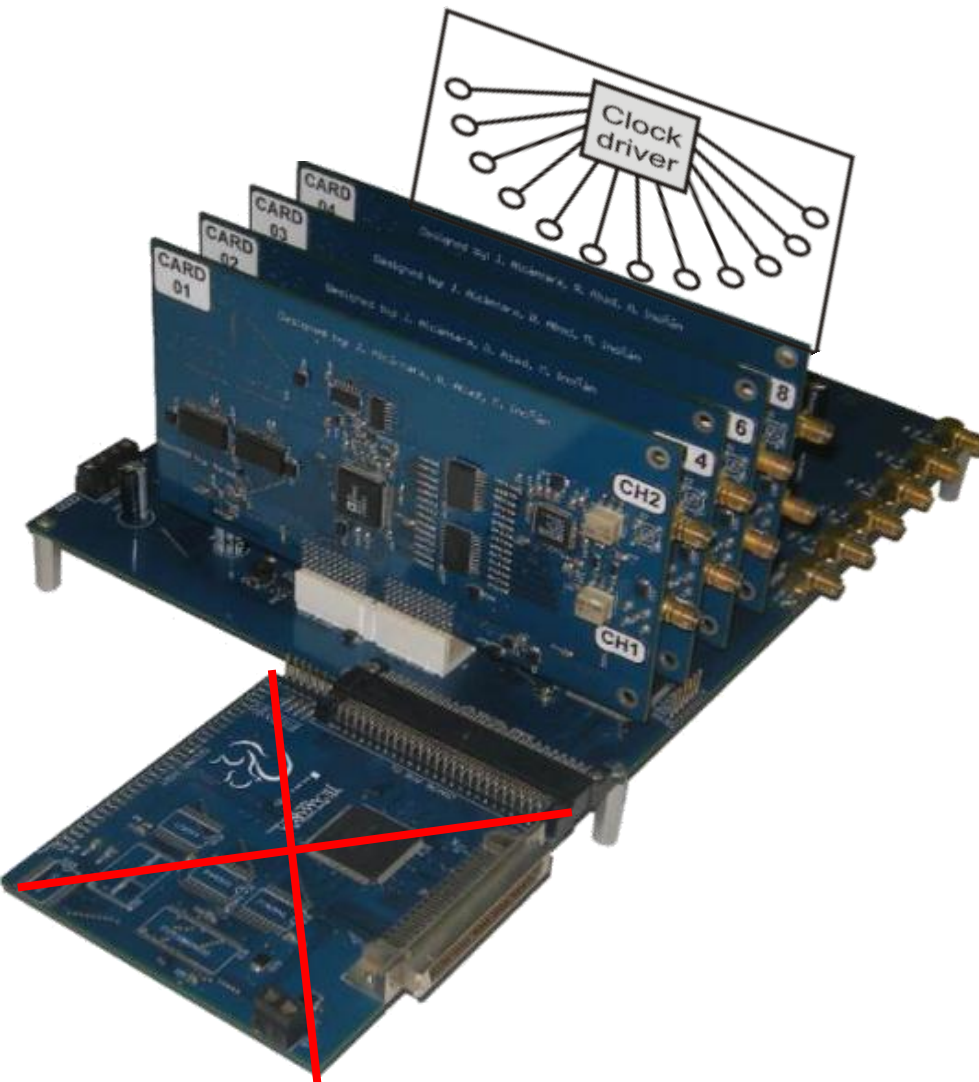
- Dynamic Range: 80dB
- Maximum transfer per channel: 1 MHz
- Decimation range: 4 to 16384
- Maximum signal level: 1.41 Vpp @ 50 ohm



# JARS 2.0



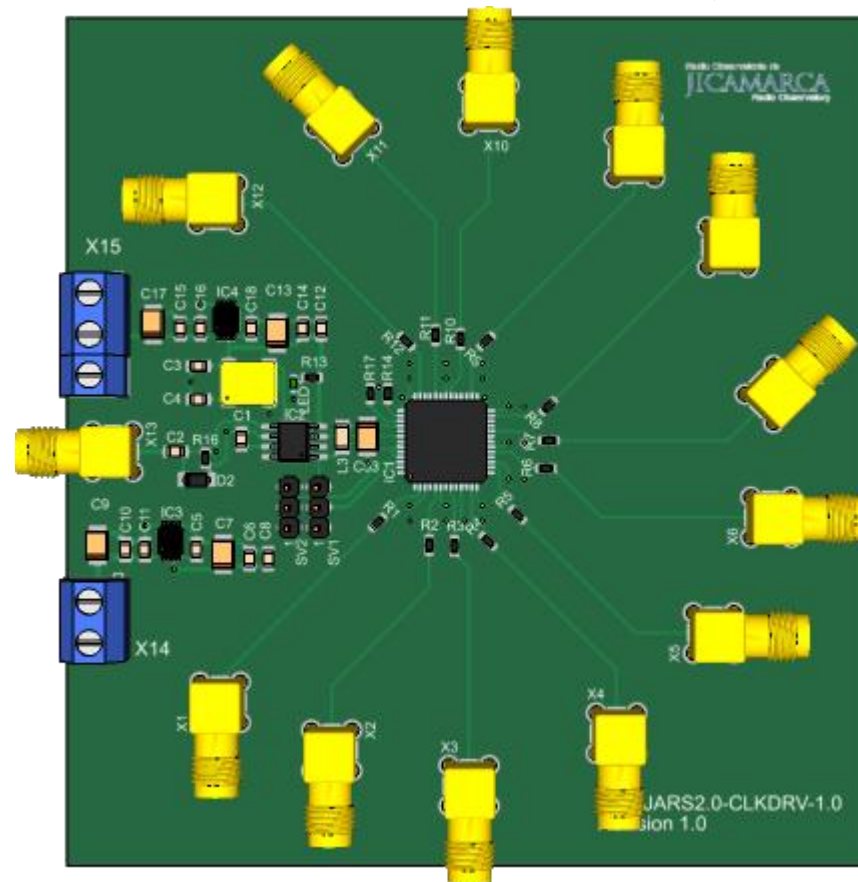
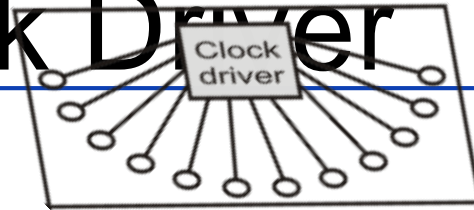
# JARS 2.0



- Avoid Proprietary technology (NiDAQ)
- OS agnostic
- Distributed clock to acquisition boards
- Better signal routing to avoid EMI
- Faster transfer rate (Gigabit Ethernet)

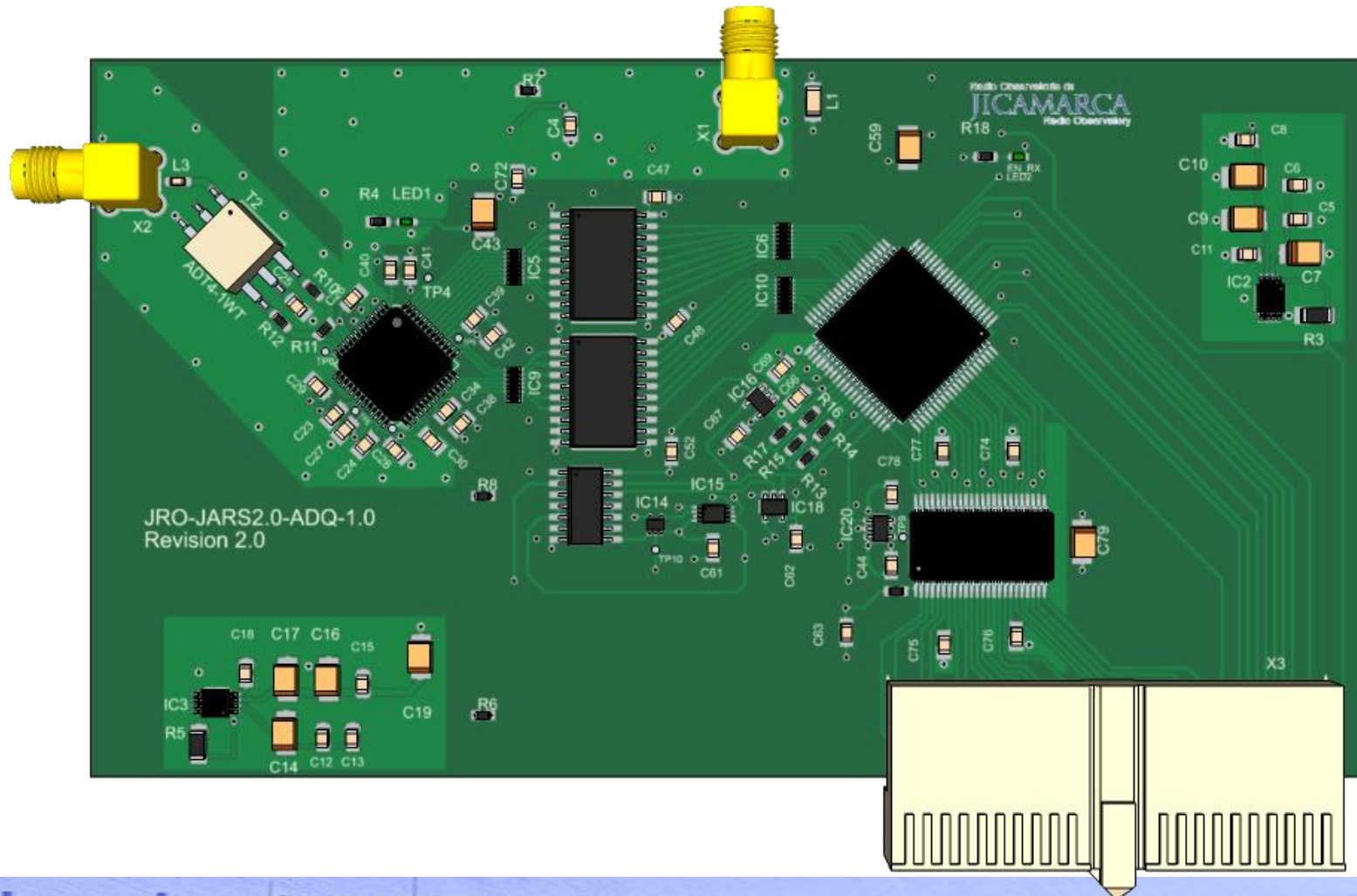


# JARS 2.0 - Clock Driver





# JARS 2.0 - Acquisition Board

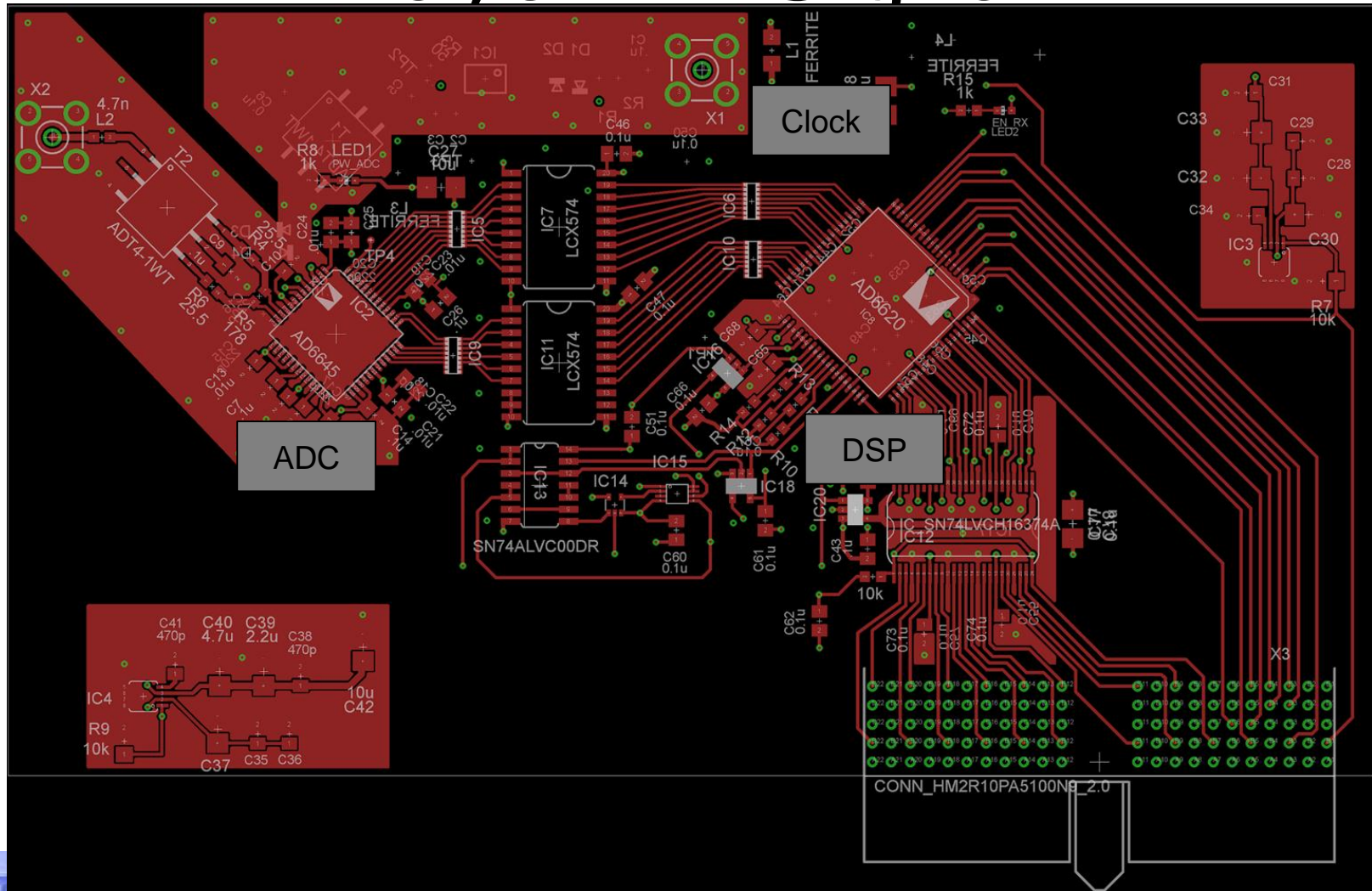




# JARS 2.0 - Acquisition Board



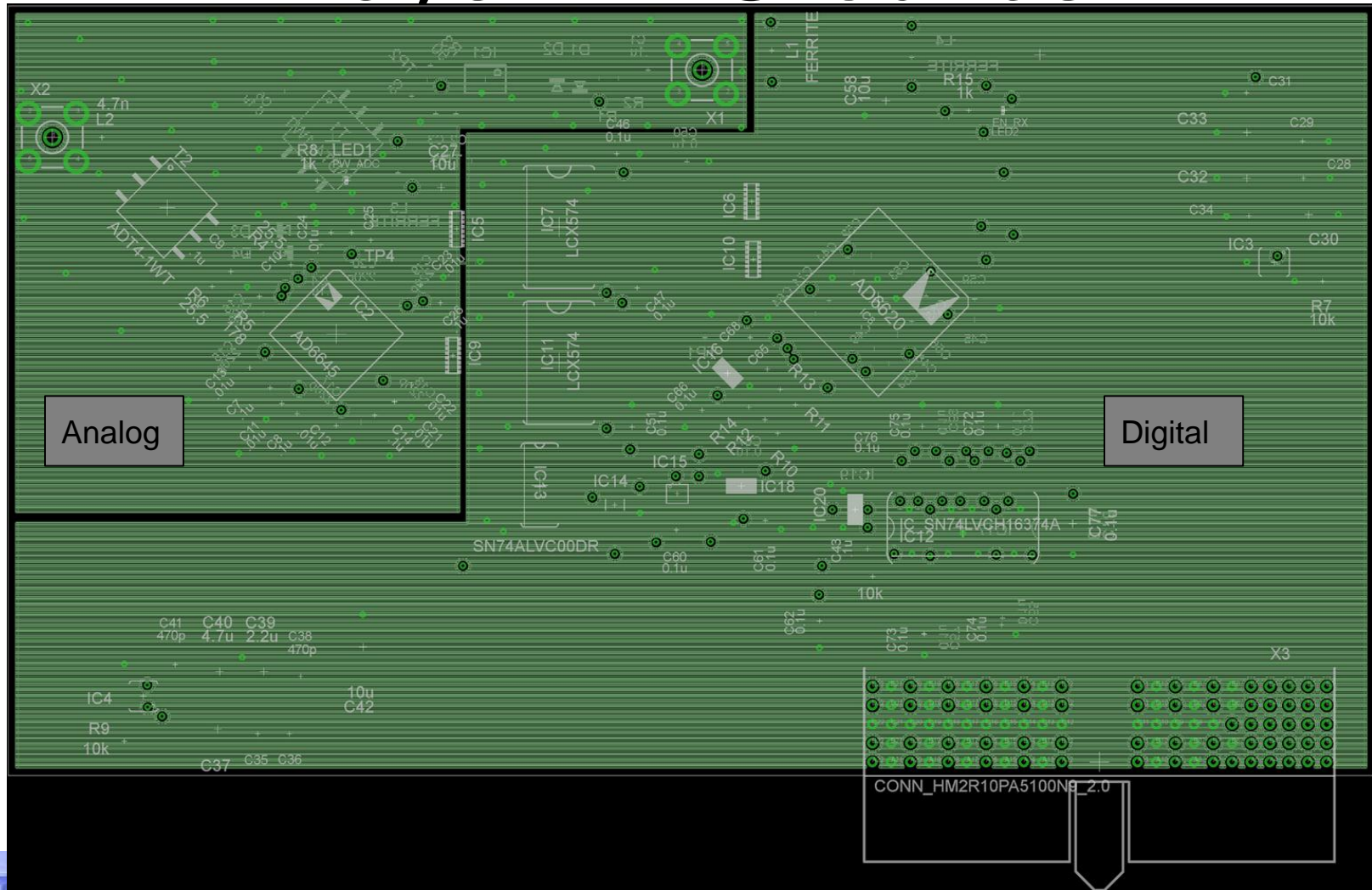
## Layer 1 - Signal



# JARS 2.0 - Acquisition Board



## Layer 2 - Grounds

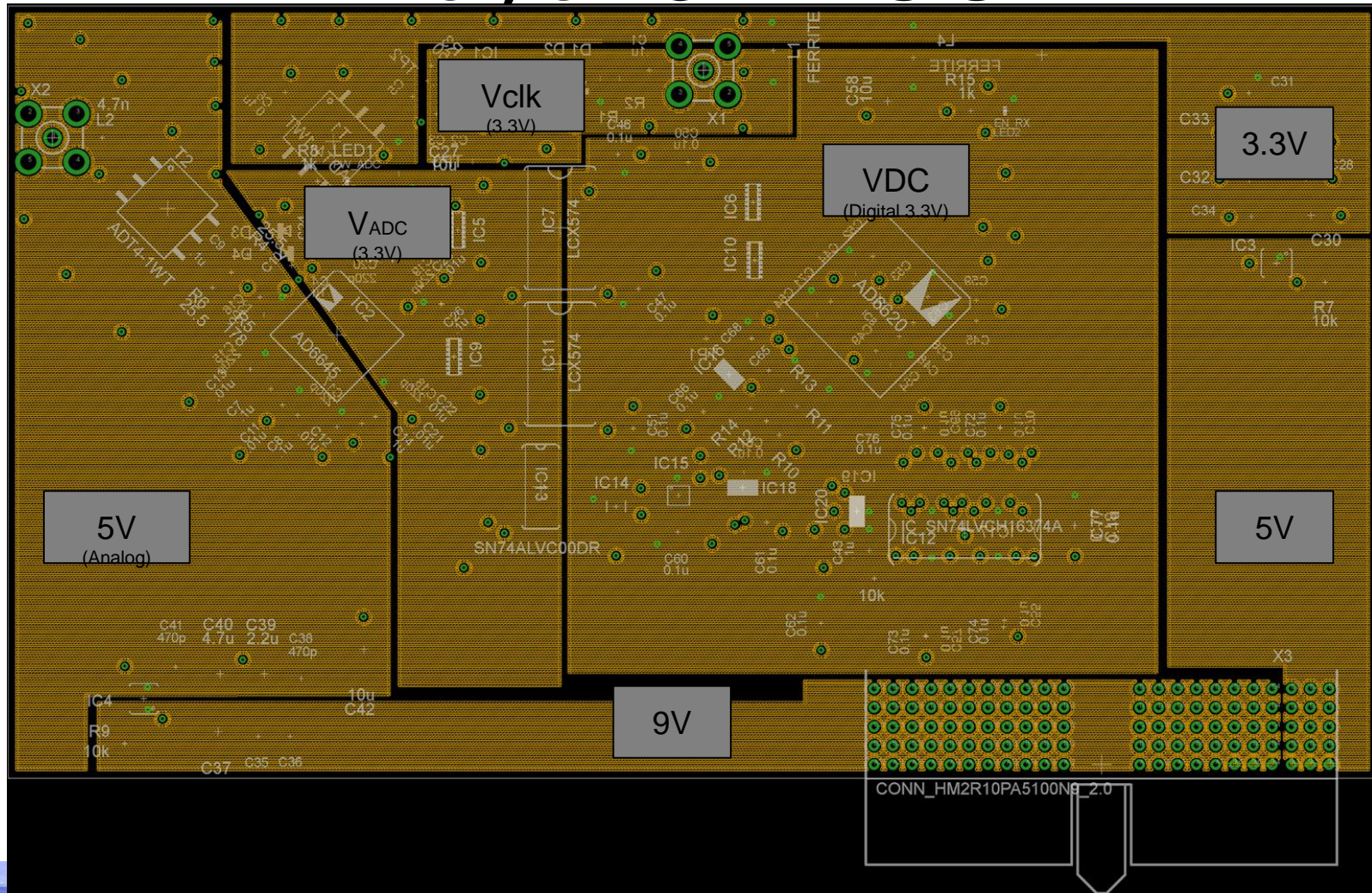




# JARS 2.0 - Acquisition Board

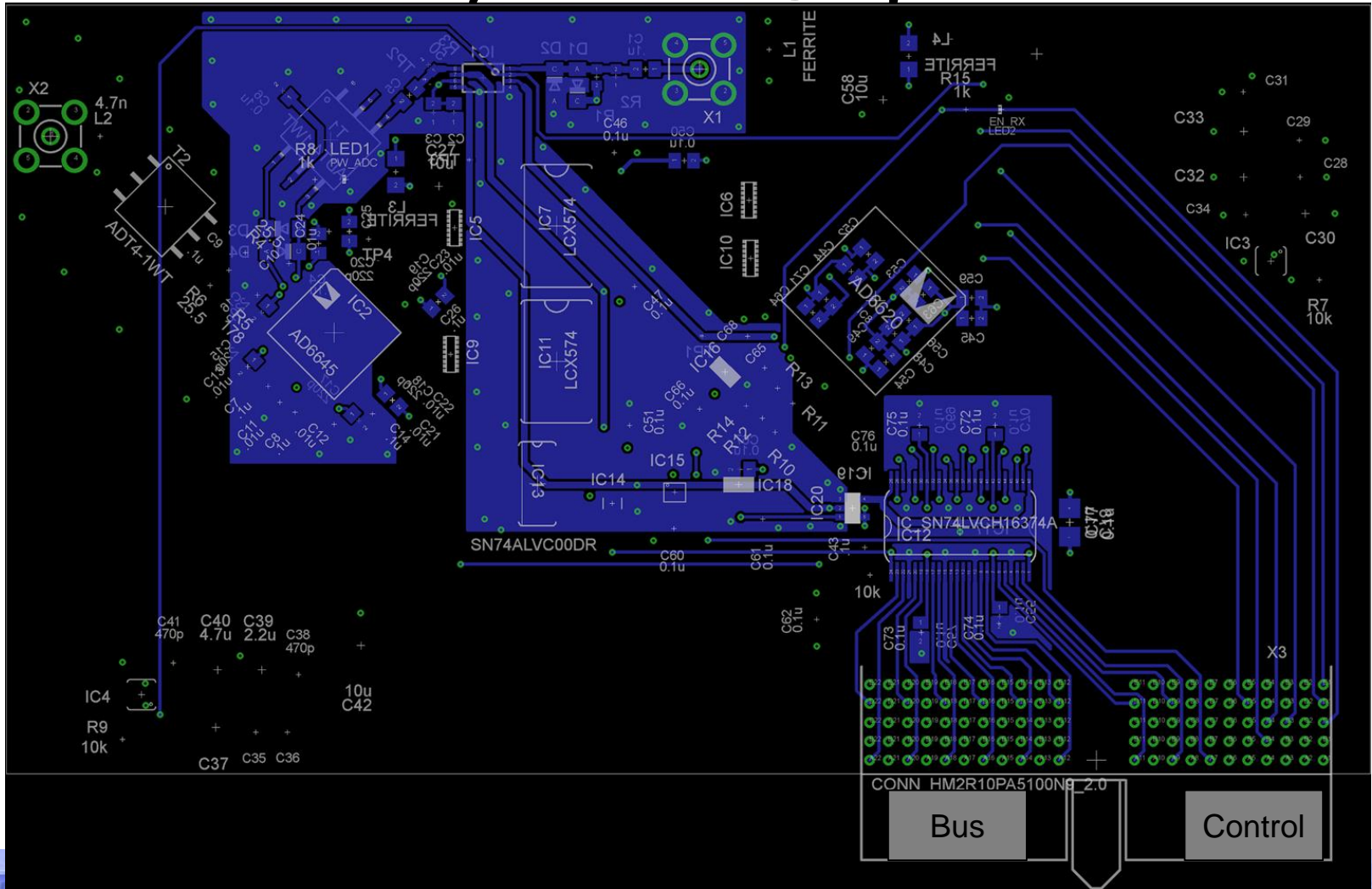


## Layer 3 - VCC

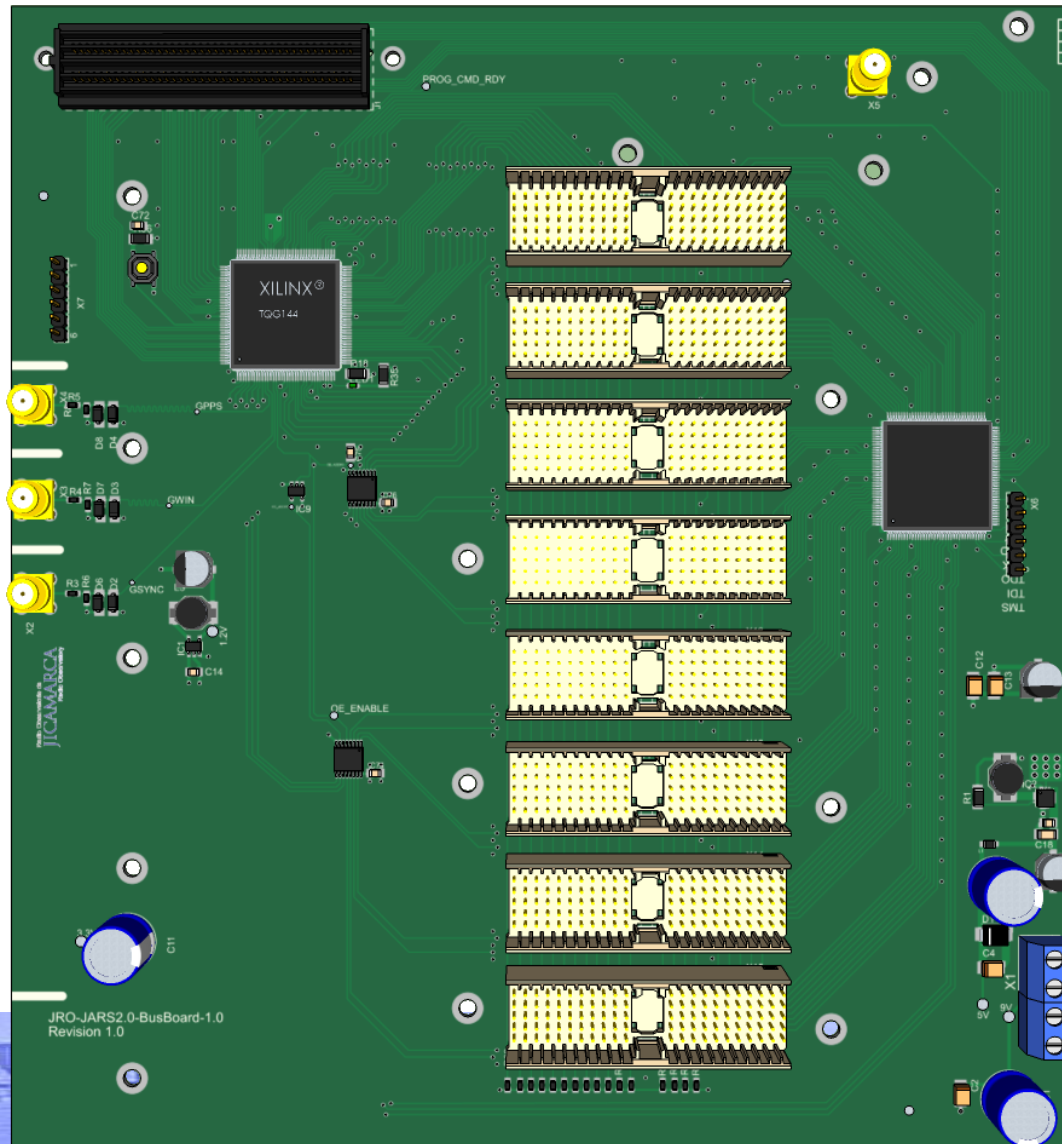




## Layer 4 - Signal

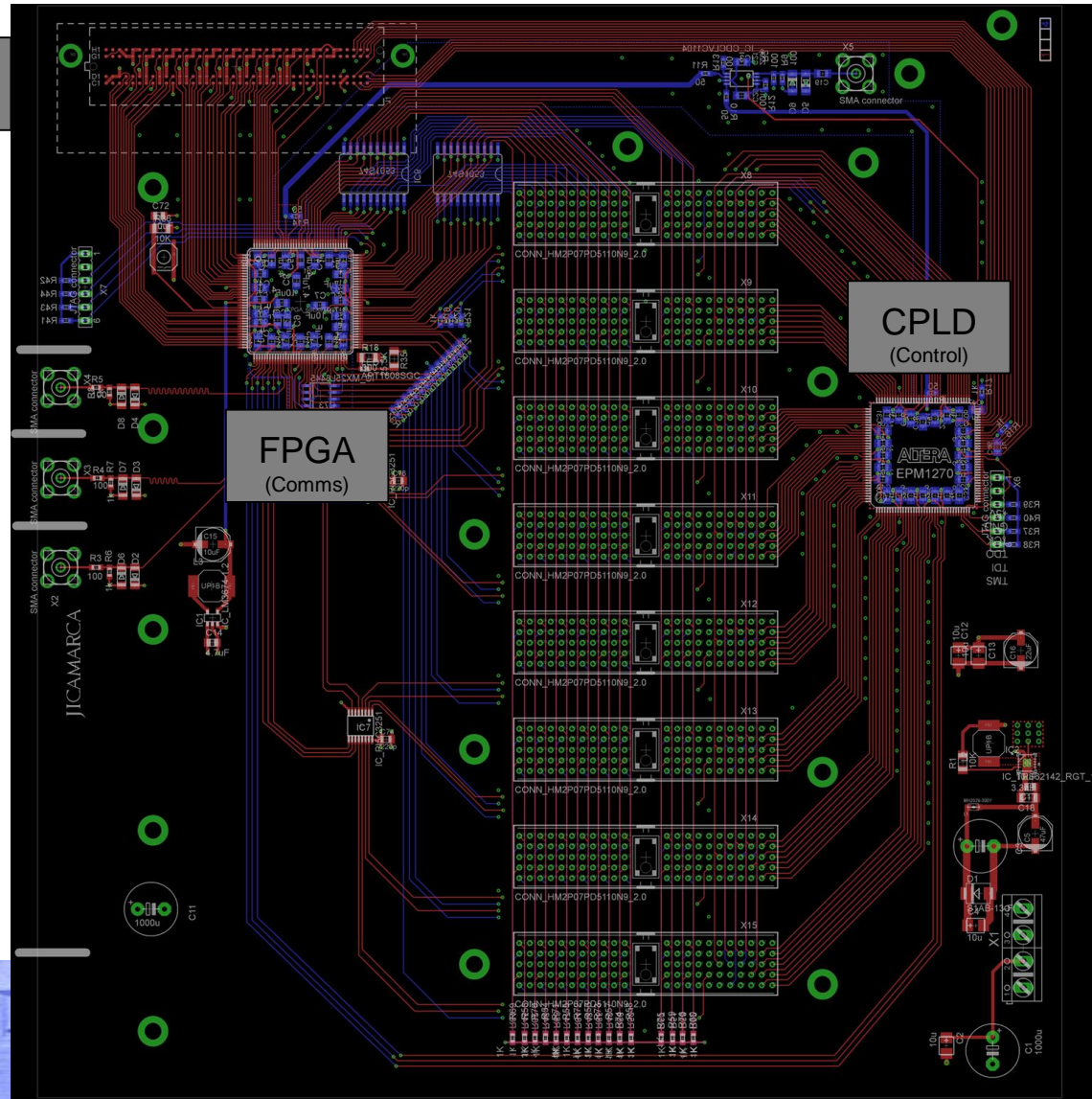


# JARS 2.0 - Bus Board



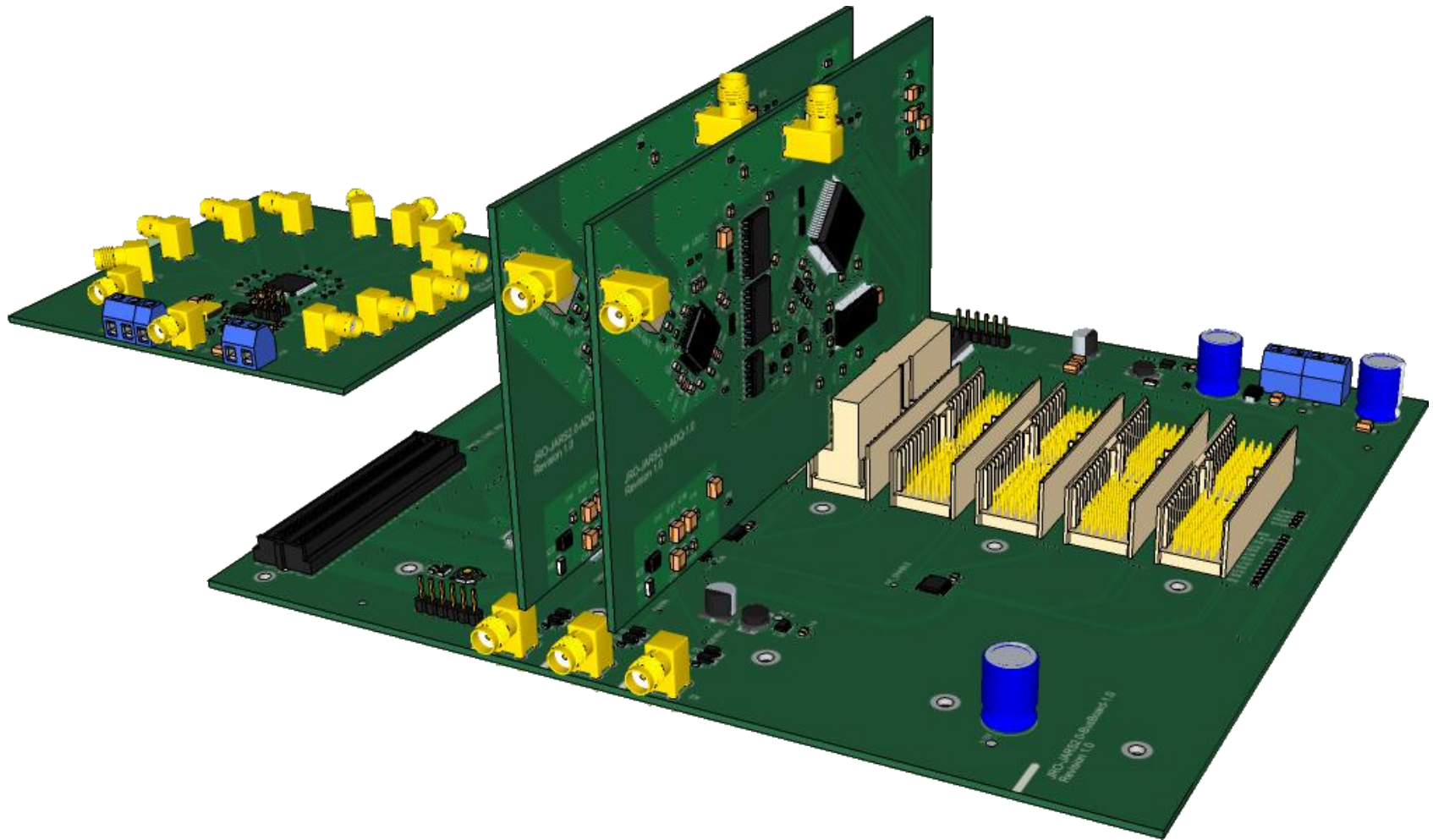
# JARS 2.0 - Bus Board

To SP601

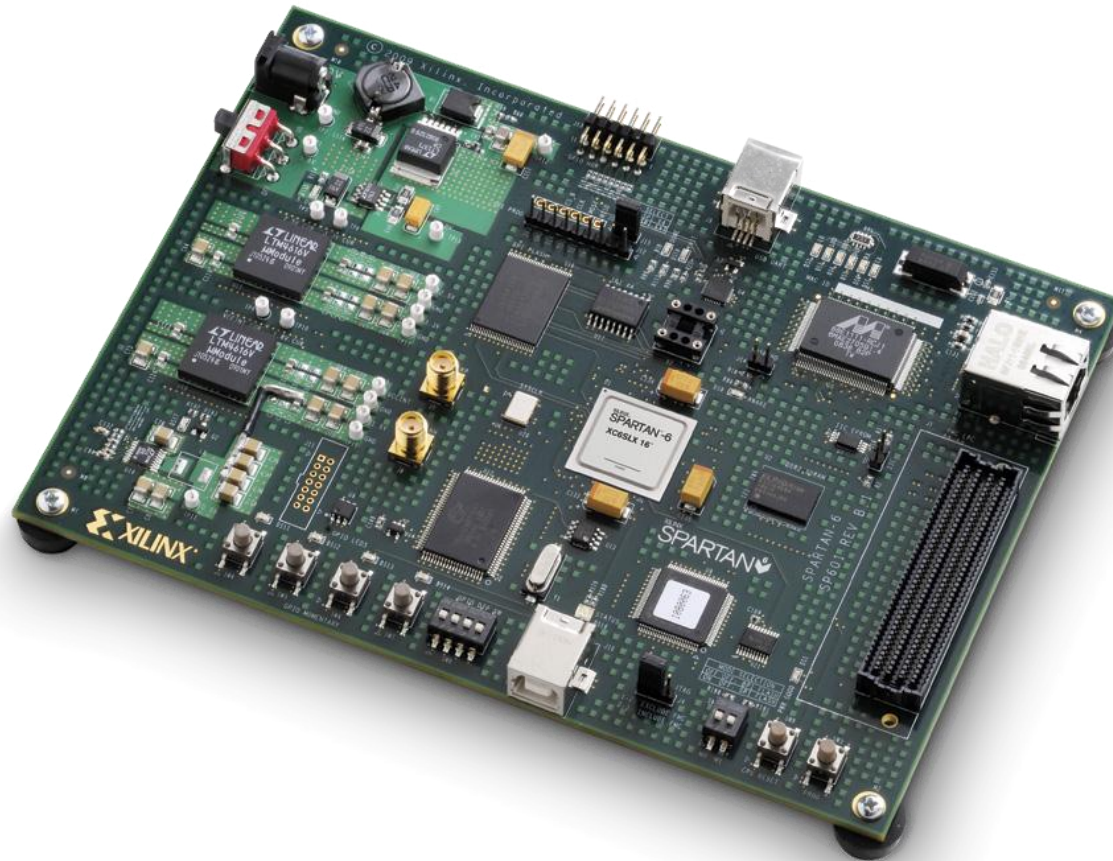




# JARS 2.0 - System



# JARS 2.0 - Control Board SP601



- Spartan 6 SP601 Board
- Gigabit Ethernet

# JARS 2.0 - Control Board

## SP601



Experiments

Hybrid2\_LP\_Faraday

Device  
Configurations

JARS: faraday

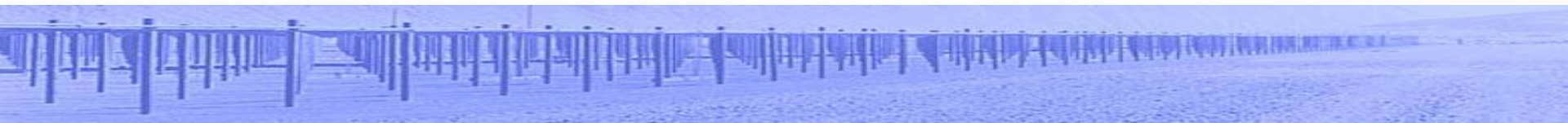
DDS: 49.92 [2016/06/13]

RC: Imaging [2016/06/21]

## JARS Configuration Details

Status	Connected
Configuration Name	JARS: faraday
Number of Cards	2
Number of Channels	4
Channels	1,2,3,4
Raw Data Directory	D:\experiments\
Process Data Directory	D:\experiments\
Data Type	FLOAT
Acquired Profiles	4095
Profiles Per Block	4096
FTP Interval	60
FFT Points	4096
Coh. Int. Stride	1
Incoherent Integrations	5
Coherent Integrations	1
filter	Filter1
# Spectral Combinations	4
Combinations	[0, 0],[1, 1],[2, 2],[3, 3],

# **Future: Integrated Radar System**



# Future: Integrated Radar System

- Web interface for users
- Real time data
- Gigabit Ethernet communication
- Flexible network topology
- Vendor-independent implementations
- Operating system independence
- Use of standard technologies to aid development (Arduino, Raspberry Pi)





# Future: Integrated Radar System

